Heterogeneous Integration for High Performance Computing, Power Electronics, and Sub-THz Wireless Applications

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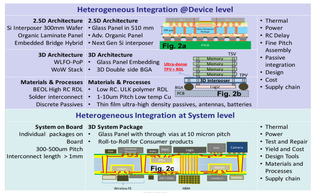
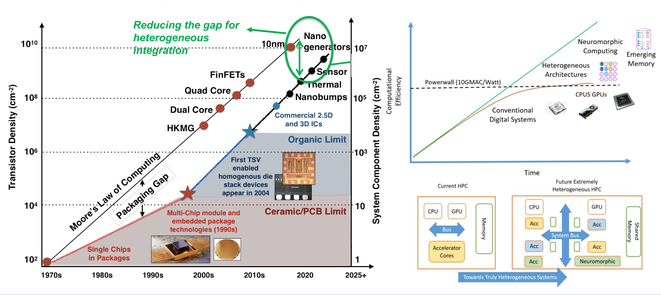
Vision

The Georgia Tech Packaging Research Center (PRC) focuses on developing AI/HPC, Power Electronics, 5G/6G and mm Wave Wireless, Flexible Electronics and Photonics systems with Thermal Solutions. Cross-disciplinary research in collaboration with 50+ global companies makes PRC a leader in system-on-package (SoP) research.

Moore's law states that transistor density doubles every year allowing for electronic systems with higher functionality and lower form factors. While transistor scaling has led the way for a new generation of multi-functional devices, it is in many ways coming to an end.



Innovations in systems packaging provides an alternative way to continue to improve performance while reducing size and develop leading edge Heterogeneous Integration technology with MCMs.



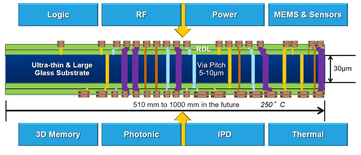
Package Evolution

With the trend toward lowering cost, decreasing thickness, and increasing I/O density, glass panel fan-out is the future in micropackaging.

Attributes	WLP	WLFO	Organic Panel Fan-out	Inorganic Panel Fan-out
Substrate	No Substrate	Molding Compound	Laminate	Glass, Poly-Si, Metal
Chip Assembly	None	None	None	None
I/O Density	Very Low	Low-Medium	Low-Medium	High
IC & Pack. Size	Small	Medium	Medium	Small-Large

Why glass?

- Ultra short interconnect lengths and miniaturized design
- High temperature stability and hermetic reliability
- Low loss and great insulating properties
- Minimum warpage and high surface smoothness



Challenges of fan-out:

- Warpage
- RDL scaling and dielectric loss
- Board-level reliability
- EMC shrinkage and electrical loss
- Thermal stability and heat management
- Outgassing
- Die placement accuracy and die-shift

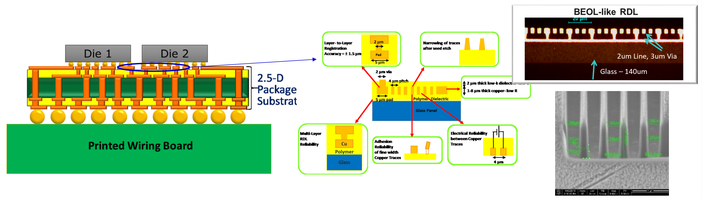
Critical Material Properties

- Low K (and Low Dielectric Loss) materials
- Processability
  - Thickness
  - Lamination, Spin-coating, Die-coating and other casting methods
- Adhesion to Copper plated substrates
  - Substrates
  - Adhesion promoters: Peel test, High temperature stability
- Surface Planarity of Films
  - Low surface roughness
  - Filler size
  - Fly cut
- Mechanical Reliability
  - Warpage of Films: Symmetric and Asymmetric Structures
  - Residual stress
- Coefficient of Thermal Expansion (CTE)
- Electrical Reliability
  - Moisture absorption
  - Leakage current
  - Elelctrochemical migration
    - Barrier layer materials

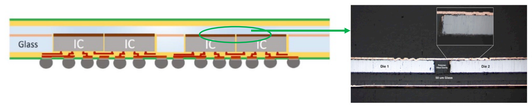
Parameters	Epoxy	Polyimide (PI)	Polybenzoxazole (PBO)	Benzocyclobutene (BCB)	Advanced Fluoropolymer
Dielectric Constant (At 1 GHz)	3.1	3.2	2.9	2.65	2.6
Young's Modulus (GPa) (at 25°C)	4	3.5	2.2	2.9	2.4
Tensile Strength (MPa) (at 25 °C)	93	200	170	87	100
% Elongation to Break	5	45	100	8	28
Coefficient of Thermal Expansion (CTE) (in ppm/K from 25-150°C)	46	35	60	42	60
Moisture Absorption (wt.%)	1.1	1.1	1.5	< 0.2	< 0.4
Curing Temperature	180°C/ 1 hr	350°C/ 1 hr	200-250°C/ 1 hr	250°C/ 1 hr	190°C/ 2 hrs
Adhesion to Copper	Excellent	Good	Good	Poor	Poor

2.5D Glass Interposer BGA

Design and demonstrate a power efficient, higher bandwidth, lower-cost and higher reliability large body size 2.5D glass interposer as Next Generation to Si interposer

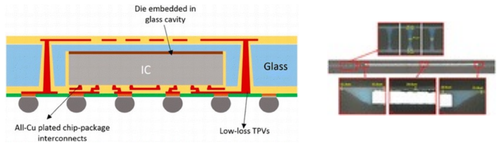


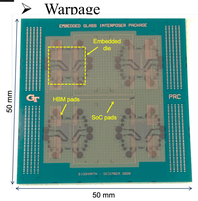
2.5D and 3D Glass Panel Embedding (GPE)



Design and demonstrate high bandwidth at low, weight, and power enabled by glass fan-out packaging

- ➢ Die shift
- ➢ Warpage



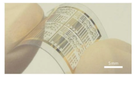


Flexible Electronics and Photonics

Flexible Electronics

- Printable & Flexible Electronics
- 3D/Inkjet/Screen printing
- Biocompatible polymers and nanomaterials
- Emerging Bio/RF/Consumer Applications
- Current activities through Nextflex

Courtesy: Schott AG

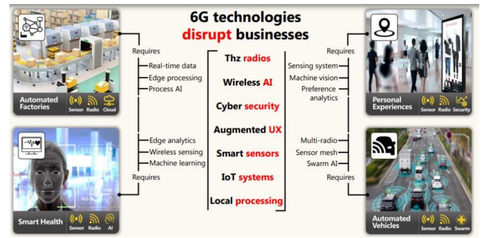


Photonics Packaging

- Optical interconnection with ultra-high data rates (e.g., 10's of Tbps)
  - Ultra-low power consumption (100 aJ/bit)
  - Very large device density
- Optical information processing of RF and mm-wave signals
- Automotive-LIDAR

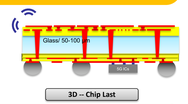
5G/6G and mm-wave

- 5G is around the corner
- What comes next?
- Applications emerging that require much higher data rate than 5G
  - MIMO, Imaging, Non-destructive testing and Virtual reality
- Trend towards Sub-THZ frequencies expected
  - 0.1-1 THz
- Requires Advanced Materials, Substrates and Package Integration Technologies



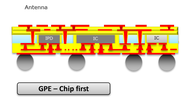
Performance

- Low-loss thin-film dielectrics
- Short vertical interconnects from embedded ICs to antennas and surface assembled components
- High performance actives and passives
- Ultra-high bandwidth antenna



Miniaturization

- 50um-100um thick core - Z shrinkage
- Double-side active and passives integration with TPVs
- Direct glass package to board assembly

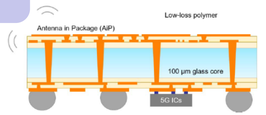


Low Cost

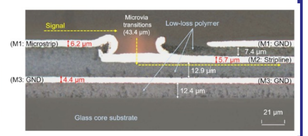
- Large-area panel manufacturing
- Double-side panel-level fabrication and assembly

Reliability

- CTE-matched glass – Zero device stress
- Excellent dimensional stability – Low warpage
- High-throughput reliable TPVs

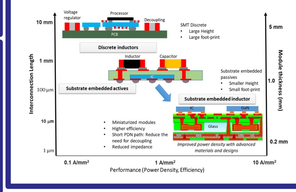


Cross-section image of 3D glass-polymer 5G modules



Side view of the cross-sectioned transmission lines and microvias transitions designed for the 28 GHz band

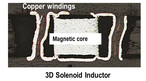
Power Electronics

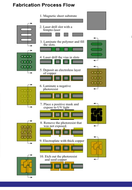


Substrate-Embedded Inductors

- Different inductor topologies have been modeled and fabricated to be embedded into the package: 2D planar, 3D solenoid and toroid
- Substrate-compatible, high-density, thin power inductors with low DC resistance (<10mΩ)

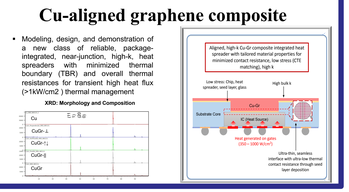
Metrics	Objectives	2D Planar	3D Solenoid
Inductance	10 nH/mm²	11 nH/mm²	7 nH/mm²
DC resistance	5 mΩ	5 mΩ	200 mΩ
Power handling	1-2 A/mm²	0.36 A/mm²	3 A/mm²
Thickness	500 μm	500 μm	500 μm





Cu-aligned graphene composite

- Modeling, design, and demonstration of a new class of reliable, package-integrated, near-junction, high-k, heat spreaders with minimized thermal boundary (TBR) and overall thermal resistances for transient high heat flux (>1kW/cm2) thermal management



Interconnects and Assembly

High-temperature Lead-free Solders

- AuSn, AuGe

→ *Cost, high bonding temperatures*

Solid-state Bonding

Direct Cu-Cu w/surface activation

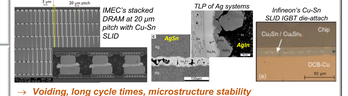
Cu-Au ultrasonic bonding

Au-Au ultrasonic / TCB bonding

→ *Manufacturability, cost*

TLP / SLID Bonding

Transient Liquid Phase / Solid-Liquid Interdiffusion

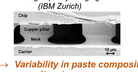


→ *Voiding, long cycle times, microstructure stability*

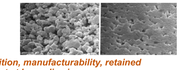
Sintering

- Nanoscale for densification at low temp. / pressure

Nanocopper ink: self-assembly using capillary bridging (IBM Zurich)



Nanosilver paste: IGBT die-attach (Semikron) before

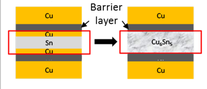


after

→ *Variability in paste composition, manufacturability, retained porosity, stress management at large die size, …*

Metastable SLID

Barrier layers isolating metastable phase



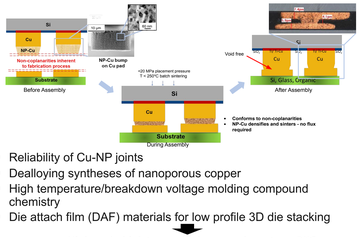
- Void-free interface
- <1min transition time
- High current-carrying capability at 10^5A/cm²
- Thermal stability >>250° C
- Superior shear strength & reliability

3D IC, high temp., high power

Cu-Cu Bonding via NanoPorous (NP) Cap

New focus

Manufacturable Chip to Substrate (C2S) assembly



- Reliability of Cu-NP joints
- Dealloying syntheses of nanoporous copper
- High temperature/breakdown voltage molding compound chemistry
- Die attach film (DAF) materials for low profile 3D die stacking

High perf., high temp., high power, low-stress PKG

Why PRC?

The semiconductor industry has identified heterogeneous integration using advanced packaging to continue microelectronics scaling and system miniaturization. The PRC represents the #1 Academic Center focused on packaging around the globe. Get involved in leading edge research and education that can shape the future of semiconductors.

Acknowledgements: GT-PRC Consortium Members